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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,519	12/19/2003	Chao-Shi Chuang	ATIP0003USA	1518

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NORTH AMERICA INTERNATIONAL PATENT OFFICE (NAIPC)
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EXAMINER	
BHAT, ADITYA S	
ART UNIT	**PAPER NUMBER**
2863	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,519	CHUANG ET AL.	
	Examiner	Art Unit	
	Aditya S. Bhat	2863	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) *1-8 and 15-22* is/are pending in the application.

4a) Of the above claim(s) *9-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8,15-20 and 22* is/are rejected.

7)☐ Claim(s) *7 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 9-14 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on May13, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-8, 15-20 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Nelson et al. (USPUB 2002/0075080).

With regards to claim 1, Nelson et al. (USPUB 2002/0075080) teaches a method for automatically calibrating the frequency range of a phase-lock loop (PLL), the method comprising:

providing a loop filter for accumulating charge to generate a loop-filter voltage; (Page 1, Paragraph 0015) (Refer to figure 1)

providing a voltage controlled oscillator (VCO) having a plurality of frequency ranges, the VCO receiving the loop-filter voltage and generating an output signal having a frequency according to the loop-filter voltage and a currently selected VCO frequency range; (Page 1, Paragraph 0005)

connecting an input of the loop filter to a control voltage; (Page 1, Paragraph 0006) and

selecting an optimal VCO frequency range by comparing the frequency of a PLL feedback signal for a plurality of the VCO frequency ranges with the frequency of a reference signal, the PLL feedback signal being generated according to the VCO output signal. (Page 1, Paragraph 0005)

With regards to claim 2, Nelson et al. (USPUB 2002/0075080) teaches a feedback divider for generating the PLL feedback signal according to the VCO output signal. (Page 1, Paragraph 0016)

With regards to claim 3, Nelson et al. (USPUB 2002/0075080) teaches a optimal VCO frequency range comprises either a first VCO frequency range or an adjacent second VCO frequency range such that the frequency of the PLL feedback signal is faster than the frequency of the reference signal for the first VCO frequency range and the frequency of the PLL feedback signal is slower than the frequency of the reference signal for the second VCO frequency range. (Page 2, Paragraph 0018)

With regards to claim 5, Nelson et al. (USPUB 2002/0075080) teaches the input of the loop filter is connected to a maximum voltage or a minimum voltage and selecting the optimal VCO frequency range further comprises conducting a linear search starting from a lowest or a highest VCO frequency range and proceeding until the optimal VCO frequency range is found. (Page 2, Paragraph 0024)

With regards to claim 6, Nelson et al. (USPUB 2002/0075080) teaches the input of the loop filter is connected to a medium voltage and selecting the optimal VCO

frequency range further comprises conducting a binary search starting from a middle VCO frequency range and proceeding until the optimal VCO frequency range is found. (Page 2, Paragraph 0024)

With regards to claim 8, Nelson et al. (USPUB 2002/0075080) teaches finding the first VCO frequency range comprises mapping a divide factor of a feedback divider to a predicted first VCO . T frequency range. (Page 1, Paragraph 0016)

With regards to claim 15, Nelson et al. (USPUB 2002/0075080) teaches phase lock loop (PLL) comprising:

a loop filter for accumulating charge to generate a loop-filter voltage; (Page 1, Paragraph 0015) (Refer to figure 1)

a VCO having a plurality of frequency ranges, the VCO receiving the loop-filter voltage and generating an output signal having a frequency according to the loop-filter voltage and a currently selected VCO frequency range; (Page 1, Paragraph 0005) and

calibration logic for selecting an optimal VCO frequency range, wherein during PLL calibration, the input of the loop filter is connected to a constant voltage, and the calibration logic searches for an optimal VCO frequency range by comparing the frequency of a PLL feedback signal for a plurality of the VCO frequency ranges with the frequency of a reference signal, the PLL feedback signal being generated according to the VCO output signal.

With regards to claim 16, Nelson et al. (USPUB 2002/0075080) teaches a feedback divider for generating the PLL feedback signal according to the VCO output signal.

With regards to claim 17, Nelson et al. (USPUB 2002/0075080) teaches a frequency detector receiving the PLL feedback signal and the reference signal, and wherein the optimal VCO frequency range comprises either a first VCO frequency range or an adjacent second VCO frequency range such that the frequency of the PLL feedback signal is faster than the frequency of the reference signal for the first VCO frequency range and the frequency of the PLL feedback signal is slower than the frequency of the reference signal for the second VCO frequency range. (Page 1, Paragraph 0006)

With regards to claim 19, Nelson et al. (USPUB 2002/0075080) teaches a switch for selectively connecting the input of the loop filter to a maximum voltage or a minimum voltage depending on a control signal from the loop controller, and wherein during PLL calibration the calibration logic conducts a linear search starting from a lowest VCO frequency range and proceeding until the optimal VCO frequency range is found. (Page 2, Paragraph 0022)

With regards to claim 20, Nelson et al. (USPUB 2002/0075080) teaches a switch for selectively connecting the input of the loop filter to a middle voltage, and wherein during PLL calibration, the calibration logic conducts a binary search starting from a middle VCO frequency range and proceeding until the optimal VCO frequency range is found. (Page 2, Paragraph 0024)

With regards to claim 22, Nelson et al. (USPUB 2002/0075080) teaches: a storage unit storing a plurality of predicted first VCO frequency ranges indexed by divide factors for the feedback divider; wherein during PLL calibration, the calibration logic

determines the first VCO operating frequency range according lo the predicted first VCO frequency range retrieved from the storage unit according lo the divide factor of the feedback divider. (Page 2, Paragraph 0032)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson (USPUB 2002/0075080) in view of Shibahara et al (USPUB 2003/0042985).

With regards to claim 4 and 18, Nelson et al. (USPUB 2002/0075080) does not appear to disclose synchronizing the PLL feedback signal with the reference signal.

Shibahara et al (USPUB 2003/0042985) teaches synchronizing the PLL feedback signal with the reference signal. (Page 9, Paragraph 0099)

It would be obvious to one skilled in the art at the time of the invention to modify the invention taught by Nelson et al to include the synchronization step in order to optimizing currents flowing in the VCO. (Page 1, Paragraph 0008, lines 8-9)

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter: Claims 7 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claims 7 and 21:

The primary reason for the allowance of claims 7 and 21 is the inclusion of the method steps of: the optimal VCO frequency range comprises the first VCO frequency range when the time duration between the second rising edges of the reference signal and the PLL feedback signal for the first VCO frequency range is shorter than that of the second VCO frequency range, otherwise comprises the second VCO frequency range when the time duration between the second rising edges of the reference signal and the PLL feedback signal for the second VCO frequency range is shorter than that of the first VCO frequency range. It is this/these features found in the claim(s), as they are claimed in the combination that has not been found, taught or suggested by the prior art of record, which makes this/these claim(s) allowable over the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Delbo et al. (USPN 6,816,019) teaches a method of automatically calibrating a phase locked loop system, Jansson (USPN 6,323,736) teaches a method and apparatus for calibrating a frequency adjustable oscillator in an integrated circuit device, Huang et al (USPN 6,741,109) teaches a method and apparatus for switching between input clocks in a phase locked loop, Nelson et al. (USPN 6,552,618) teaches a

VCO gain self calibration for low voltage phase lock loop applications and Groe et al. (USPN 6,856,205) teaches VCO with automatic calibration.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aditya S. Bhat whose telephone number is 571-272-2270. The examiner can normally be reached on M-F 9-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Barlow can be reached on 571-272-2269. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Aditya Bhat
June 10, 2005

John Barlow
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